

SP8630

600MHz÷10

The SP8630 is an asynchronous emitter coupled logic divider which provides an ECLIII/10K compatible output when used with an external pulldown resistor. It requires an AC coupled input of 600mV p-p.

FEATURES

- ECL Compatible Outputs
- AC-Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 350mW
- Temperature Range: -30°C to +70°C

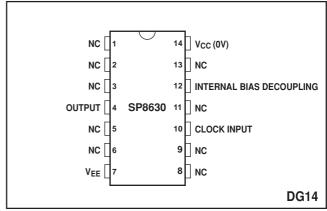


Fig. 1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

$\begin{array}{ccc} \text{Supply voltage, V}_{\text{EE}} & -8\text{V} \\ \text{Output current} & 15\text{mA} \\ \text{Storage temperature range} & -65^{\circ}\text{C to } +150^{\circ}\text{C} \\ \text{Max. junction temperature} & +175^{\circ}\text{C} \\ \text{Max. clock input voltage} & 2\cdot5\text{V p-p} \end{array}$

ORDERING INFORMATION

SP8630 B DG 5962-92003 (SMD)

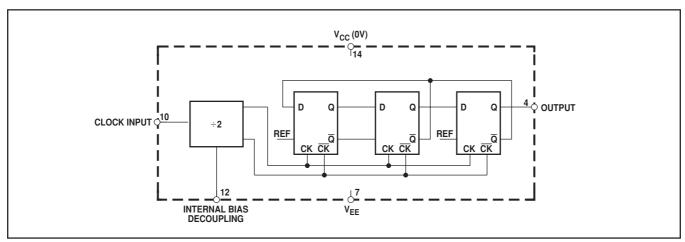


Fig. 2 Functional diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, the Electrical Characteristics are guaranteed over specified supply, frequency and temperature range Supply voltage, V_{CC} = 0V, V_{EE} = $-5\cdot 2V\pm 0\cdot 25V$ Temperature, T_{AMB} = -30° C to $+70^{\circ}$ C

Characteristic	Symbol	Value			0	Notes
		Min.	Max.	Units	Conditions	Notes
Maximum frequency (sinewave input)	f _{MAX}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f _{MIN}		40	MHz	Input = 400-800mV p-p	
Power supply current	I _{EE}		70	mA	$V_{EE} = -5.2V$	
Output low voltage	V _{OL}	−1.8	−1.5	V	$V_{EE} = -5.2V$	3
Output high voltage	V _{OH}	-0.85	−0.7	V	$V_{EE} = -5.2V$	3
Minimum output swing	V _{OUT}	400		mV	$V_{EE} = -5.2V$	

NOTES

- 1. The temperature coefficients of $V_{OH} = +1.63 \text{mV/}^{\circ}\text{C}$, and $V_{OL} = +0.94 \text{mV/}^{\circ}\text{C}$ but these are not tested. 2. The test configuration for dynamic testing is shown in Fig.5.
- 3. Tested at 25°C only.

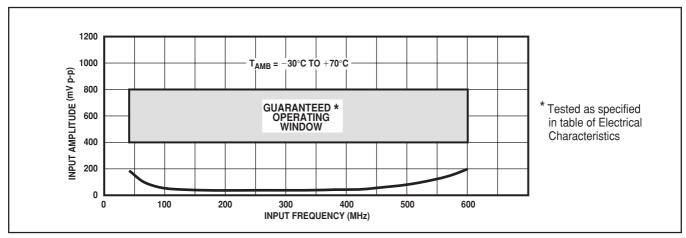


Fig. 3 Typical input characteristic

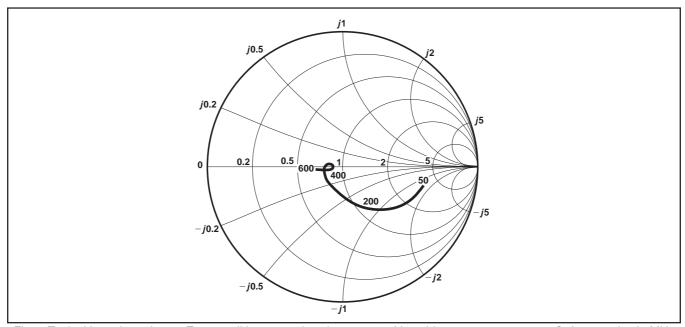


Fig. 4 Typical input impedance. Test conditions: supply voltage = -5.2V, ambient temperature = $25^{\circ}C$, frequencies in MHz, Impedances normalised to 50Ω

OPERATING NOTES

- 1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground. 2. The circuit will operate down to DC but slew rate must be better than $100V/\mu s$.
- 3. The output is compatible with ECLII. There is an internal load of $3k\Omega$ at the output. The output can be interfaced to ECLIII/10K by the addition of $1.5k\Omega$ to the output to increase the output voltage swing.
- 4. Input impedance is a function of frequency, see Fig. 4.
- 5. All components should be suitable for the frequency in use.

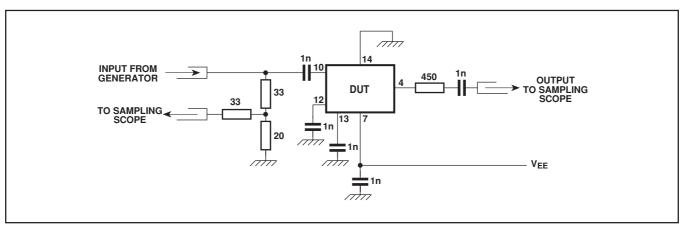


Fig. 5 Test circuit

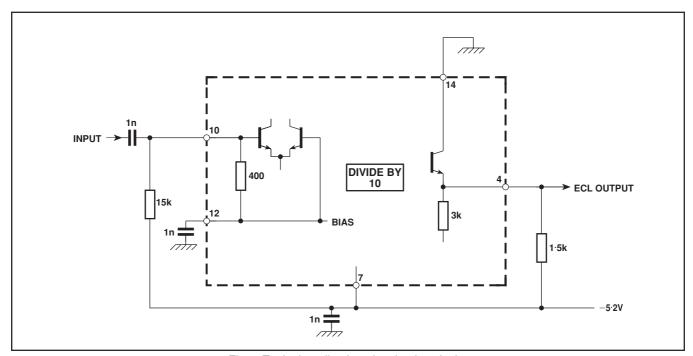
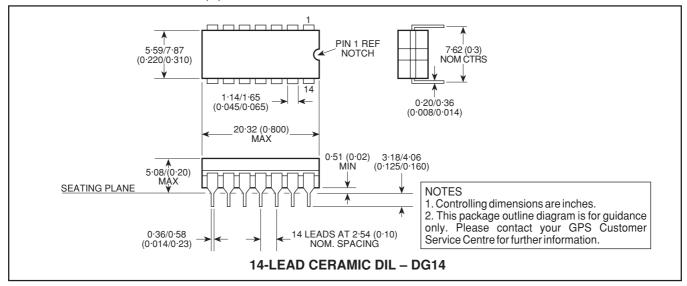


Fig. 6 Typical application showing interfacing

PACKAGE DETAILS

Dimensions are shown thus: mm (in).





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